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LOW AREA HIGH SPEED COMBINED MULTIPLIER USING MULTIPLEXER BASED FULL ADDER

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Abstract:- In Digital Image Processing, Median Filter is used to reduce the noise in an image. The median filter considers each pixel in the image and replaces the noisy pixel by the median of the neighbourhood pixels. The median value is calculated by sorting the pixels. Sorting in turn consists of comparator which includes adders and multiplier. Multiplication is a fundamental operation in arithmetic computing systems and is used in many DSP applications such as FIR Filters. The adder circuit is used as a main component in the multiplier circuits. The Carry Save Array (CSA) multiplier is designed by using the proposed adder cell based on multiplexing logic. The proposed adder circuit is designed by using Shannon theorem. The multiplier circuits are schematised and their layouts are generated by using VLSI CAD tools. The proposed adder based multiplier circuits are simulated and results are compared with CPL and other circuit designed using Shannon based adder cell in terms of power and area and the intermediate state involved in the circuit is eliminated. The proposed adder based multiplier circuits are simulated by using 90nm feature size and with various supply voltages. The Shannon full adder circuit based multiplier circuits gives better performance than other published results in terms of power dissipation and area due to less number of transistors used in Shannon adder circuit.

Keywords: *Half adder, Array multiplier, Booth's Multiplier, Vedic Multiplier, Vedic Mathematics.*

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I INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry .The need for low power has caused a major paradigm shift in circuit design. In recent years, power is being given as much importance as area and performance. In applications such as personal computing devices and wireless communications system, average power consumption is a critical design concern. The cost associated with packaging and cooling such device is significantly high. Since core power consumption must be dissipated through the packaging, increasingly expensive packaging and cooling strategies are required. Unless power consumption is dramatically reduced, the resulting heat will limit the feasible packing and performance of VLSI circuits and systems. Consequently, there is a clear financial advantage to reducing the power consumed in high performance systems. Pass-transistor logic is reported as one of the alternative logic that can enhance circuit performance. Since, signal can propagate using both the source and the gate; its high functionality can reduce the number of transistors in terms of multiplexing control input technique. Since, a PTL based circuit can consist of only one type of MOS transistor therefore, it has a low node capacitance and as a result CPL enables high-speed and low-power circuits. In this paper, Carry Save Array (CSA) multiplier is used for designing multiplier circuit. This multiplier is constructed by using 4 different adder cells namely proposed adders, Shannon, CPL techniques. The CSA multiplier is constructed using AND gates, half adder,

and full adder blocks. The half adder is designed using pass transistor logic which utilizes EX-OR and AND gates, which is shown in Fig.1. The 1-bit multi operand addition can be extended to an n-bit multi operand addition by cascading the CSA operators. The multiplier is schematised by DSCH3 CAD tool and its layout is generated by Microwind 3 VLSI CAD tool. We have analyzed the basic circuits and proposed adder based multiplier circuits in terms of power dissipation and area and observed better performance in our proposed Shannon based multiplexing logic circuit

II LITERATURE SURVEY

Rapidly growing technology has raised demands for fast and efficient real time digital signal processing applications. Multiplication is one of the primary arithmetic operations every application demands. A large number of multiplier designs have been developed to enhance their speed. Active research over decades has lead to the emergence of Vedic Multipliers as one of the fastest and low power multiplier over traditional array and booth multipliers. Honey Durga Tiwari.et.al talked about designing a multiplier and square architecture is based on algorithm of ancient Indian Vedic Mathematics, for low power and high speed applications. They explained Urdhvatiryakbhyam and Nikhilam algorithm and found that Urdhvatiryakbhyam, is applicable to all cases of multiplication but due to its structure, it suffers from a high carry propagation delay in case of multiplication of large numbers. This problem has been solved by introducing Nikhilam Sutra which reduces the multiplication of two large numbers to the multiplication of two small numbers. Prof J M Rudagil.et.alldesigned a multiplier using vedic mathematics. They explained Urdhvatiryakbhyam and found that it is efficient Vedic multiplier with high speed, low power and consuming little bit wide area was designed. It was also found that the multiplier based on vedic sutras had execution delay of almost half of that of binary multiplier. Sree NivasA .et.all presented a technique that modifies the architecture of the Vedic multiplier by using some existing methods in order to reduce power. They explained Nikhilam sutra and double base number system. Nikhilam sutra method is not valid for negative numbers. They found that Vedic Multiplier without any Modification has high power consumption. Vedic Multiplier with modified Two's complement block has less power consumption with cost of delay and area. Full adders are designed for a 16-bit vedic multiplier to decrease number of slices and delay. The results obtained are compared and it is found that the reformed full adders have less delay. The design is implemented using four adders of different techniques such as full adder using two half adders and an OR gate. Second modified full adder is designed by using XOR gate and 2:1 multiplexer, third modified full adder by using two 4:1 multiplexer and fourth modified full adder using a combination of XOR gate, XNOR gate and a 2:1 multiplexer. After comparing the results, they concluded that the third modified full adder has better performance [3]. Gate diffusion input (GDI) is a method used for describing the structure of low-power digital combinatorial circuit. Consumption of power, delay that is produced and complexity of the circuit are reduced using this technique; thereby it maintains less complexity in logical layout. The GDI technique is implemented using two transistors for a deep range of complex logic design [4]. A high speed 32-bit vedic multiplier is designed. For addition of partial products in a 32-bit vedic multiplier Kogge stone adder and a ripple carry adder is used. Two multipliers are implemented using these two methods and results are compared with these two multipliers [5]. In 8-bit multiplier which is implemented using Urdhva Tiryagbhyam sutra, the partial product addition is realized using carry skip technique. A digital processor requires a multiplier as it is a basic block in the processor [6]. A 32-bit vedic multiplier is proposed using one carry save adder. The input of multiplier is arranged in two 16-bit numbers to apply it stepwise using Urdhva Tiryagbhyam sutra and the partial product is added using one carry save adder thus reducing the hardware blocks in the circuit [7]. The processors are integrated into one chip as demand of complex processors is increased. But the load on the processor is not reduced. To reduce this load, the main processor is equipped with co-processors [8]. Design of a hybrid FIR filters using vedic multipliers and fast adders is todays need in many DSP processors. FIR filters play a significant role in the field of digital signal processors to eliminate noise suppression in electro cardio graph, imaging devices and the signal stored in analog media. So filter evaluation is accomplished to reduce the noise level. Multipliers and adders play a vital role in determining the performance of FIR filter. They have proposed modified Annuprya vedic multiplier methods with Kogge Stone fast adder for implementation in the direct form FIR filter [9]. Multipliers play a major role in today's digital signal processing and various other applications. Both signed and unsigned multiplications are required in many computing applications.

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III PROPOSED SYSTEM

The multiplier is constructed by using adder cell. The CSA multiplier building block is containing half adder and full adder circuit. The half-adder circuit is designed by using multiplexing method, which is shown in Fig.1. The power dissipation and area are reduced due to multiplexing method. The MCIT techniques reduce the number transistor than CMOS design techniques. The proposed Shannon full adder circuit as shown in Fig.2 combines the multiplexing operation for the sum operation and the Shannon Theorem for the carry operation; the sum and carry circuits are designed based on Standard full adder equations. An input C and its complement are used as the control signal of the sum circuit. The two-input X-OR gate is developed using the multiplexer method. The output node of the two-input multiplexer circuit is the differential node. According to standard full adder equation, the sum circuits need three inputs. In order to avoid increasing the number of transistors due to the addition of a third input, the following arrangement is made, the CPL X-OR gate multiplying with C's complement input and EX-NOR gate is multiplied with input C, and thereby reducing the number of transistors in the sum circuit. The carry for the half adder is given by,

Half Adder
Carry=A.B

Shannon's Theorem
Carry= (A.B) + (B.B')

Full Adder
Sum = A xor B xor C
Sum= ((A xor B).C') + ((A xor B)'.C)
Carry= (A.B) + (B.C) + (C.A)
Carry= (A+B) C + (A.B)

Existing Adder
Carry= (A+B) C + (A.B)+(B'.C')

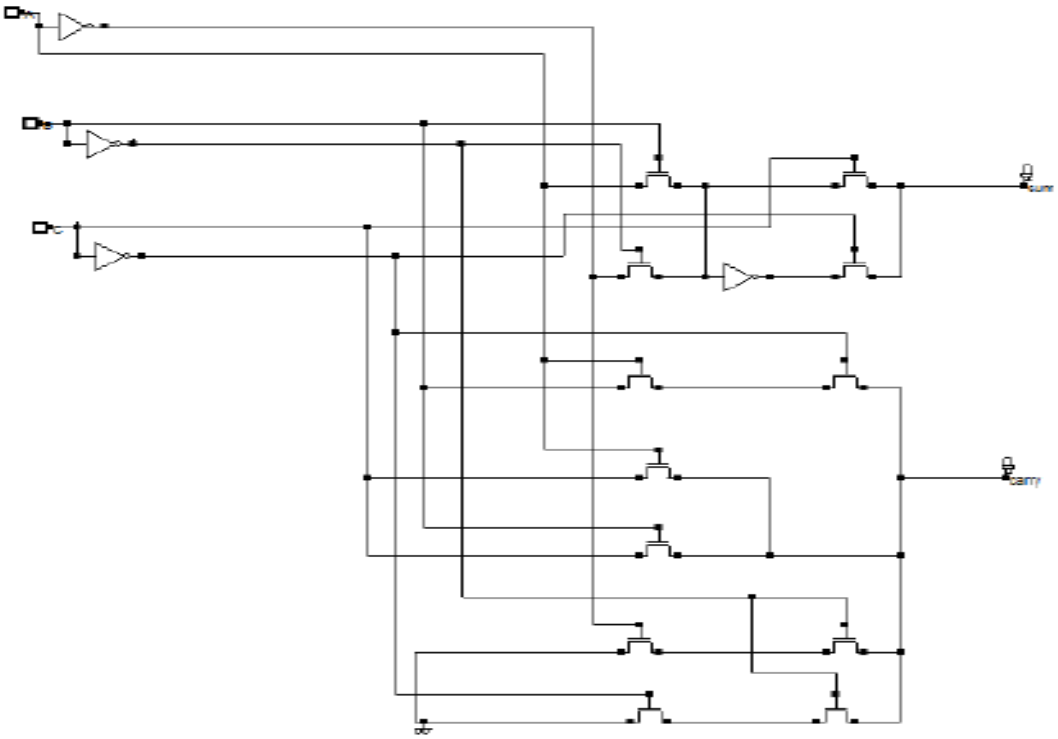

Fig 1 Proposed adder cell

TABLE I
TRUTH TABLE OF FULL ADDER

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

C and *C'* node is called the differential node of the circuit. Two complementary (*C* and *B*) inputs are used in the full adder carry circuit for balancing the circuit and to avoid the floating wire concept. In this circuit, all of the pass inputs are connected at VDD line so that the pass gates are always on. The control input terminals are connected to the function inputs. In the proposed adder 2, from Table I instead of giving all the inputs from external input the internal output from the SUM circuitry acts as input to the carry logic. From the truth table it can be found that when A XOR B output is one, the value of Cout is equals to C. When it is zero, the value of Cout is equals to the value of A. In this circuit, there is comparative reduction in the number of transistors and so reduction in Area and power.

Multiplier Design

In this paper, we have designed and analyzed Carry Save Array (CSA) multiplier circuit using our proposed adder cell. The design feature size is 90nm and corresponding supply voltage is 1.2V. The Carry save Array (CSA) multiplier is a linear array multiplier as shown in Fig.3. The linear multiplier propagates data down through the array cell. Each row of CSAs adds one additional partial-product to the partial sum. As the operand size increases, linear arrays grow at a rate equal to the square of the operand size because the number of rows in the array is equal to the length of the multiplier, and the width of each row is equal to the width of multiplicand.

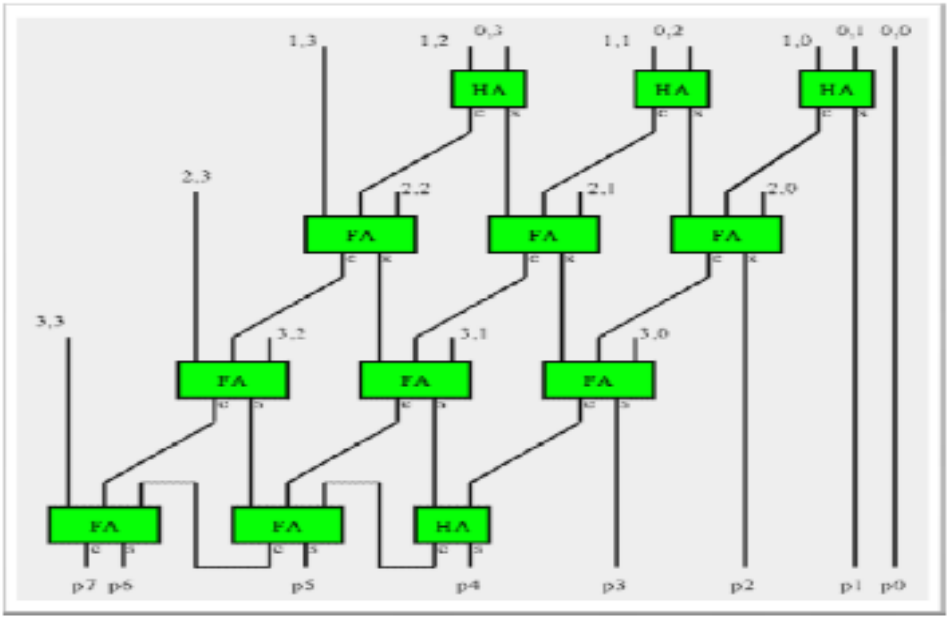

Fig 2. Carry save Array (CSA) Multiplier

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IV SIMULATION RESULTS AND DISCUSSION

In the multiplier array, a full adder with balanced carry and sum delays is desirable because the sum and carry signals are in the critical path. The speed and power of the full adder are very important for large arrays. The 8x8 bit multiplier circuits were simulated with a BSIM4 layout model .We compared the simulated results of our proposed 1-bit adder cell with existing author's results which shows better performance in terms of power dissipation and area. Our proposed 1- bit adder cell consumes less power, and less area than the various Technology Schematic proposed 1-bit adder cells, due to regular arrangement of transistor tree structure, less critical path and multiplexing method of designs. The only drawback of our proposed adder cell is that it occupies larger area. From the simulated results it is clear that the multiplier circuits designed based on the proposed adder cell gives better performance in terms of power, area than the CPL-based adder cell. The main reason for the lower propagation delay of Shannon-based multipliers is that they are balanced in the carry circuits.

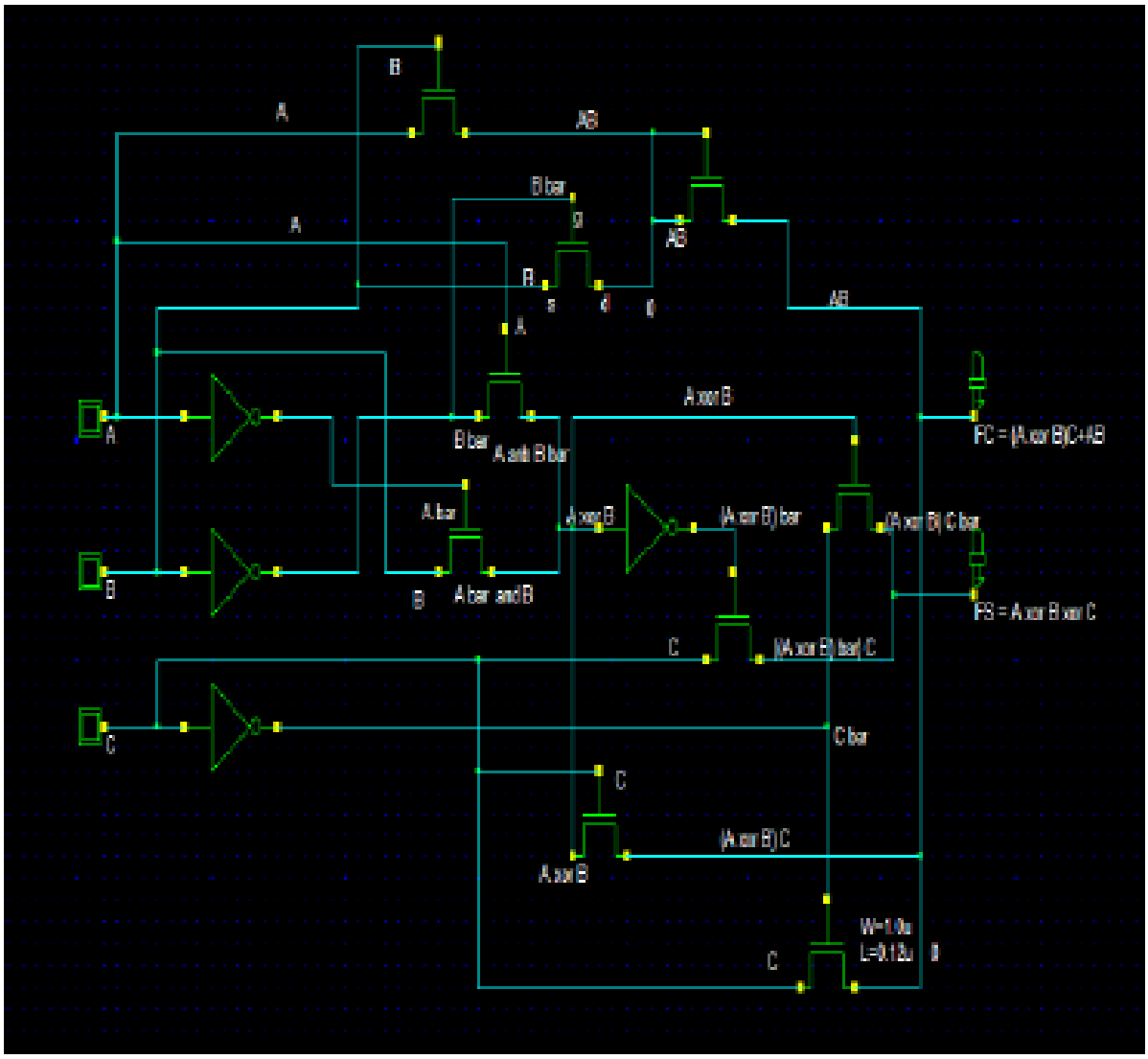

Figure 3. RTL schematic of multiplier

Area

```
Device and node counts:
                MOSFETs -        9
   MOSFET geometries -        2
     Voltage sources -        4
         Subcircuits -        0
   Model Definitions -        2
     Computed Models -        2
   Independent nodes -       16
      Boundary nodes -        6
         Total nodes -       22
```

Delay

```
Parsing                          0.02 seconds
Setup                            0.06 seconds
DC operating point               0.05 seconds
Transient Analysis               0.03 seconds
Overhead                         0.46 seconds
-----------------------------------------------
Total                            0.62 seconds
```

Power

```
Power Results

VVoltageSource_1 from time 0 to 100
Average power consumed -> 4.401984e-015 watts
Max power 3.733690e-004 at time 6.1e-008
Min power 0.000000e+000 at time 0
```

V .CONCLUSION

The Shannon adder based CSA multipliers circuits are simulated by using Microwind 3 VLSI CAD tools and parameter values are analyzed by using BSIM 4 analyzer. The circuits were compared with existing circuits. Shannon adder based multiplier gives better performance than existing circuits in terms of power dissipation and Area. The proposed multiplier circuits can be used in the low power application of VLSI circuits In this paper, power dissipation and area of the multiplier using the proposed adder cell is compared with other multipliers designed using existing adders and used in Digital image Processing. Further it can be used in applications such as FIR filter, FFT, Rank Order Filters where adders and multipliers plays a major role.

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