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DESIGN OF AREA EFFICIENT WALLACE TREE MULTIPLIER WITH ADVANCED DATA COMPRESSORS

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Abstract:- This paper presents the design of 15- 4 compressor using 5-3 compressors as basic module. Four different types of approximate 5-3 compressors are used in a 15-4 compressor for less power consumption and high pass rate. We have analyzed the results in all the cases. A 16 × 16 bit multiplier is simulated using the proposed 15-4 compressor. Simulation results show that the multipliers with proposed approximate compressors achieve significant improvement in power as compared to the multipliers with existing 15-4 compressor. Area of the proposed multipliers are low as compared to other existing approximate multipliers.

Keywords: *Wallace tree multiplier, 15-4 compressor, 4 bit parallel adder, Xilinx, 5-3 compressor.*

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I INTRODUCTION

Basic requirements for VLSI design are low power consumption. Compareness of design and speed, reduced area will improve portability, low power will improve reliability and if the delay is reduced speed is increased. Arithmetic units are the essential blocks of digital systems such as digital signal processor, Microprocessor, Microcontroller and other data processing units. Multiplier is the substantive part of the electronic device and decides the overall performance of the system [1]. When designing a multiplier, huge amount of power and delay are generated. To minimize these disadvantages, adders and compressor are used. Hence reducing delay in multiplier has been a main aim to enhance the performance of the digital systems like DSP processors [8]. Hence many attempts are done on multipliers to make it faster. It is an effective hardware realization of digital system that is nothing but a Wallace tree which multiplies two numbers and minimizes the number of partial products [4]. Multipliers have three phases - generation of partial products, reduction of partial products and final stage In vector processors, several multiplications are performed to obtain data or loop level parallelism. High processing speed and low power consumption are the major advantages of this multiplier.

II LITERATURE SURVEY

Approximate Adders for Approximate Multiplication

Record The opening between limits of CMOS advancement scaling and prerequisites of future application extraordinary jobs that needs to be done is developing quickly. There are a few promising course of action moves toward that together can decrease this opening all around. Assessed figuring is one of them and beginning late, has pulled in the most grounded idea of standard researchers. Actuated figuring mishandles regular blunder nature of businesses and highlights predominant hugeness helpful programming and equipment use by compromising computational quality (e.g., exactness) for computational endeavors (e.g., execution and centrality). Reliably, two or three exploration attempts have investigated assessed setting up all through every single one of the layers of enlisting stack, in any case, most by a wide margin of the work at equipment level of thought has been proposed on adders. In [1], an overall review of cutting edge undesirable adders is given. Furthermore, it in like way gives assessment considering both standard game plan estimations and what's more assessed selecting design estimations.

Induced Multiplier by Partial Product Technique

The differing accumulated multipliers (Array, wallace and Dadda multipliers) are organized by the inadequate thing opening strategy. The divided thing puncturing technique is simply to cut any two sections from the essential halfway things made by the standard multipliers.

In the first place, we discussed the evaluated display multiplier. Show multiplier is prominent because of its essential structure. The enlargement of the multiplicand with one multiplier bit makes each partial thing. The made midway things are incorporated into the wake of moving based their bit orders. N-1 adders are required where N is the multiplier length. The figure of show multiplier is made by fragmented thing puncturing technique. (b) shows the assessed display multiplier. In light of the result examination among correct and gauge, the figure multiplier delivers the better results with respect to deferment, district and power.

III EXISTING METHOD

The inner structure of compressors avoids carry propagation. Either there are not any carry signals or they do arrive at the same time of the internal values[5-7]. For the purpose of reducing the delay in the second stage, several compressors are needed. Small sizes of compressors are useful for designing the small size multiplier. In multiplier design, the different sizes of compressors are required depending upon the bit size. In this paper, a scheme for delay reduction in 16bit Wallace tree multiplier with 15:4compressor is considered. To build 15:4compressor a 5:3compressor is considered as a basic module. AND gate is used for the generation of partial products. For ‘N’ bit multiplier ‘N2’ AND gates are required. In the partial product reduction phase, there are three major components namely half adder, full adder and 5-3 compressor[8-11]. The last stage of adding can be done by using Kogge-Stone adder Surmised compressor are utilized in thirteenth, fourteenth and15th segment of multipliers. The incomplete item decrease stage comprises of half adder, full adder and 5:3 compressor. the point when the quantities of bits in the section are 2 and 3 half adders and full adders are utilized in every segment. If there should arise an occurrence of a solitary piece, it is moved further to the resulting level of that segment with no requirement for additional handling. Until just two columns will remain, this decrease procedure is rehashed. At last, summation of the last two lines is accomplished utilizing 4-piece Kogge-Stone adder.

15-4 Compressor

A compressor is simply an adder circuit. It takes a number of equally-weighted bits, add all of them, and produces some sum signals. Compressors are normally used with the purpose of reducing and accumulating a large number of inputs to a smaller number in a parallel manner. They are the very important parts of the multiplier design as they highly influence the speed of the multiplier. Their main application is within a multiplier, where a large number of partial products have to be summed up concurrently. For high speed applications like DSP, image processing required several compressors to perform the arithmetic operation. A compressor adder provides reduced delay over conventional adders using both half adders and full adders. Here the representation as ‘N-r’, in which ’N’ denotes as the number of bits and ‘r’ denotes as the total number of 1’s present in ‘N’ inputs. The compressor reduces the number of gates and the delay with reference to other adder circuits. The inner structure of compressors avoids carry propagation. Either there are not any carry signals or they do arrive at the same time of the internal values. Compressors are largely used in the reduction stage of a multiplier to accumulate partial products in a concurrent manner. In this part it is considered the design of 15-4 compressor by using with approximate 5-3 compressors [5]. This compressor compresses 15 inputs (C0-C14) into 4 outputs (B0-B3). The 15-4 compressor consists of three phases. The first phase has five full adders, the second phase uses two 5-3 compressors and finally the 4-bit kogge stone adder.

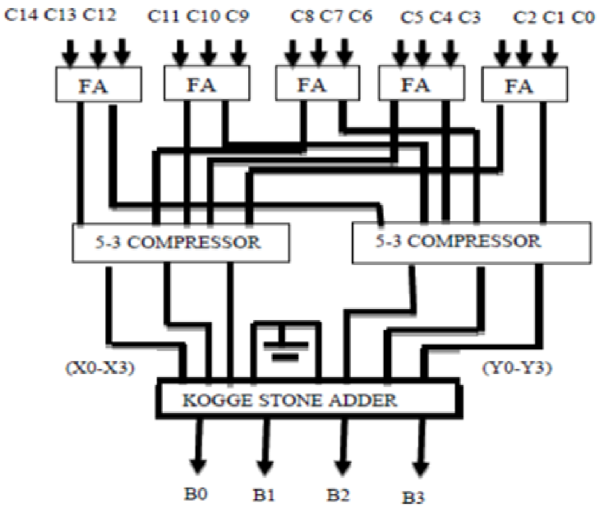


Fig 1: Logic Diagram of Approximate 15-4 Compressor

The 15-4 compressor consists of 5-3 compressor as a basic design. The 5-3 compressor utilizes five primary inputs namely A0, A1, A2, A3, A4 and produces three outputs namely B0, B1, B2. In this compressor, the presence of number of 1's at the input decides the output of compressor and also uses counter property.

The design of compression of given 5 inputs into 3 output is called the design of 5-3 compressor. Error rate of 5-3 compressor is considered. The design equations of 5-3 approximate compressor are shown in following equations respectively. The logic diagram of approximate 5-3 compressor.

$$B_2^{'} = [A_3 . A_2]$$

$$B_2 = A_0 . [\sim(A_0 \oplus A_1)] + A_2 . (A_0 \oplus A_1)[A_3 . (\sim(A_0 \oplus A_1 \oplus A_2 \oplus A_3))]$$
$$+A_4 . [A_0 \oplus A_1 \oplus A_2 \oplus A_3]$$

$$B_1 = A_0 . [\sim(A_0 \oplus A_1)] + A_2 . (A_0 \oplus A_1) \oplus [A_3 .(\sim(A_0 \oplus A_1 \oplus A_2 \oplus A_3))]$$
$$+A_4 . [A_0 \oplus A_1 \oplus A_2 \oplus A_3]$$

$$B_0 = [A_0 \oplus A_1 \oplus A_2 \oplus A_3 \oplus A_4]$$

Kogge Stone Adder

In 1973, Peter M. Kogge and Harold S. Stone presented the idea of productive and superior adder called kogge-stone adder. It is essentially an equal prefix viper. This sort of adder has the forte of quickest expansion dependent on configuration time. It is known for its uncommon and quickest expansion dependent on configuration time [9], In Fig 5, shows the kogge stone adder Prefix Adders are for the most part characterized into 3 classes

A. Pre-Processing: In this stage, generate and propagate signals are given by the equations.

Pi = Ai ⊕ Bi   Gi = Ai. Bi

B. Generation of carry: In this stage, carries are calculated with their corresponding bits and this operation is executed in parallel manner. Carry propagation and generation are used as intermediate signals. The logic equations for carry propagate and generate are shown below.

Gi = (Pi .Giprev) + Gi

Pi = (Pi . Piprev)

C. Final Processing: In final processing, the sum and carry outputs bits are computed for the given input bits and the logic equation for the final processing stage is given by

Ci = Gi

Si = Pi ⊕ Ci-1

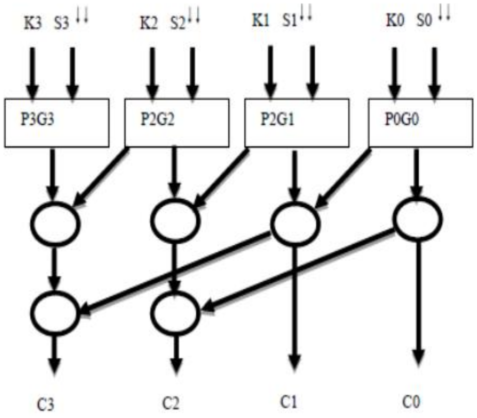


Fig 2: Block Diagram of Kogge Stone Adder

IV PROPOSED METHOD

Microprocessors and Digital Signal Processors (DSP) are playing a significant role to handle the complexity of digital signal. About 95% of the processors in the market are based on digital signal [1]. Digital signal processors take care of convolution, correlation and filtering of digital signal [2]. Multipliers, shifters and adders are mainly used to accomplish these tasks. Among the three modules, multiplier is the most complex one. Multipliers take more time and consume higher power than other two modules [3]. Multipliers have three phases - generation of partial products, reduction of partial products and final stage addition. Reducing the partial products take much time and power in the multiplier. Many techniques were proposed to reduce the critical path in the multiplier [4]-[5]. Among them, the use of compressors in partial product reduction stage is the most popular. Compressors are basic circuits which are made of full adders or half adders to count the number of "ones" in the input. Several compressors are required in this partial product reduction stage. Various compressors such as 3-2, 4-2, 5-2 and 5-3 were proposed by researchers in the last 20 years [6]-[9]. These are useful only when the size of multiplier is small. 16 × 16, 32 × 32 bit multipliers require large size of compressors. High order compressors provide better results in terms of power and speed [10]-[12]. But it consumes more area than low order compressors. Output "sum" value is calculated normally when any one of the operand value of adder is "0". When both operands are "1", "sum" value can be fixed as "1" from that bit position to least significant bit. This technique is used to minimize the error distance of the adder. Approximate XOR/XNOR adder for inexact computing is proposed by Zhixi Yang et al in [15]. Both XOR and XNOR gates are required to calculate the output of the adder. Three different approximate methods were proposed. The output expression for "sum" and "carry" is approximated. Instead of using two XOR gates, only one XNOR gate has been utilized to calculate "sum". Similarly, one XOR, one OR and two AND gates are used for "carry". Low power imprecise adder were proposed by Honglan Jiang et al in [16] where they optimized transistor count, power consumption and power delay product (PDP) of the adder. Moreover, the number of incorrect outputs of the adder is also small. In [17]-[18], accuracy, error distance and various design parameters of approximate adders are analyzed and compared. Approximation methodologies were applied in generating the partial product phase [19]. A 2 × 2 bit approximate multiplier is designed by altering the one output combination. In this technique, multiplier produces "7d" when it multiplies "11" by "11". But the actual output of the multiplier is "1001". The probability of getting error in this multiplier is 0.0625. An error has been introduced in the partial product generation phase. Adder tree (reduction tree) of this multiplier is same as accurate multiplier. Several other approximation techniques were proposed in the partial product reduction stage [20]-[27]. One need not consider the particular row of partial products when the value of multiplier bit is "0" also particular column value can be skipped when multiplicand bit is "0". technique is called row and column bypassing [20]-[21]. In [22], some of carry-save adders are skipped in both horizontal and vertical directions based on the number of zeros in the multiplier input. In [23], partial product tree is split into two parts.

Accurate multiplier became utilized in MSB side of the multiplier. No multipliers became used in LSB facet in which approximation rule turned into carried out. In [24], "n" bit multiplier was carried out by two "n/2" bit sub-multipliers. Then, maximum massive "n/2" multiplier become implemented by means of two similarly "n/4" sub multipliers and least great "n/2" multiplier become implemented by way of an approximate "n/4" multiplier. Then, all partial products are gathered by means of a Wallace tree. Compressors can cope with massive range of inputs than half of and complete adders. 4-2 compressor is widely used by numerous researchers which reduces the four partial products into partial merchandise. The opportunity of having an mistakes in approximate four-2 compressor is zero.003 which is very minimum than any inaccurate adder circuit. Two designs of approximate four-2 compressor are proposed on this paper. Design 2 of approximate four-2 compressor is the best compressor in latest days. In [28], the performance of diverse multipliers become as compared. It changed into determined that, introducing compressors within the partial production tree gives the lowest mistakes rate, minimum normalized errors distance and first rate circuit metrics. In this paper, we've proposed higher order compressor for 16 × 16 bit multiplier. Use of numerous approximate 4-2 compressors in large size multiplier reasons large errors. It is essential to get a minimal mistakes as well as decent circuit overall performance.

Designs of Approximate 5-3 Compressors

In this section, 4 designs of a 5-3 approximate compressor are offered. 5-3 compressor has 5 primary inputs (X0, X1, X2, X3, X4) and 3 outputs (O0, O1, O2). This compressor makes use of the counter belongings. Output of the compressor depends on variety of 1's present at input. This proposed compressor also referred to as 5-3 counter [11]. In this paper, we've called this module as a compressor due to the fact this module compresses five bits into three bits. We have selected 5- 3 compressor because it's far a primary module for 15-4 compressor. Error rate and Error distance of every layout are considered.

A. Design 1

In this design, initially output O2 of 5-3 compressor is approximated. Logical AND between inputs X3 and X2 matches with accurate output O2 of the conventional 5-3 compressor with an error rate of 18.75%. The following expressions show design 1 of 5-3 approximate compressor. Figure 3 shows the design1 of approximate 5-3 compressor.

$$O_2^{'} = X_3 \cdot X_2$$

$$O_2 = \left(X_0 \cdot \left(\sim(X_0 \oplus X_1)\right) + X_2 \cdot (X_0 \oplus X_1)\right)($$
$$X_3 \cdot (\sim(X_0 \oplus X_1 \oplus X_2 \oplus X_3))) + X_4 \cdot (X_0 \oplus X_1 \oplus$$
$$X_2 \oplus X_3)$$

$$O_1 = \left(X_0 \cdot \left(\sim(X_0 \oplus X_1)\right) + X_2 \cdot (X_0 \oplus X_1)\right) \oplus$$

(

$$X_3 \cdot (\sim(X_0 \oplus X_1 \oplus X_2 \oplus X_3))) + X_4 \cdot (X_0 \oplus X_1 \oplus X_2 \oplus X_3 \oplus X_4)))$$

$$O_0 = X_0 \oplus X_1 \oplus X_2 \oplus X_3 \oplus X_4$$

O0 2 is the approximated output and O2, O1, O0 are the accurate output of the 5-3 compressor. The approximated output matches with the accurate output for 26 inputs out of 32 inputs. Table 4.1 shows the error distance between approximate O 0 2 and actual output O2. In this design, only O2 is approximated and O1, O0 are same as original expression. Here, O2 and O1 have weightages of 4 and 2; the weightage of O0 is 1. In this design, the error distances for remaining 6 error cases are either 4 or -4.

minimum error distance, the output O0 of 5-3 compressor is replaced by following expression.

$$O_0' = [(X_3 \cdot X_2 \cdot (\sim X_1) \cdot (\sim(X_0)) + ((\sim X_4) \cdot X_3 \cdot X_2 \cdot (X_1 \oplus X_0)) + (X_4 \cdot X_1 \cdot X_0 \cdot (X_2 \oplus X_3))](\sim(X_3 \cdot X_2)) : (X_4 \oplus X_3 \oplus X_2 \oplus X_1 \oplus X_0)$$

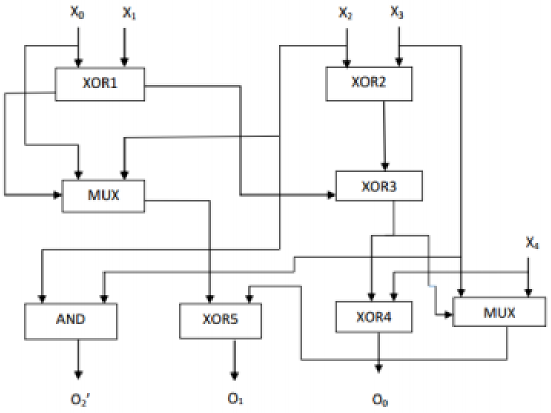


Fig 3: Approximate 5-3 Compressor (Design 1)

Finally, O1 is kept as original expression. O2 replaced by O0 2 and O0 is replaced by O0 0 to get the minimum error distance. Maximum error distance is 4 for only one input pattern (i.e. input number 12) and in the remaining five cases; the error distance is either +3 or -3. Critical path of this design is higher than accurate design. This design has additional logic gates such as one MUX and one XOR in critical path when compare to accurate design.

X[4:0]	O'_2	O_2	O_1	O_0	Error Distance
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	0	1	0
3	0	0	1	0	0
4	0	0	0	1	0
5	0	0	1	0	0
6	0	0	1	0	0
7	0	0	1	1	0
8	0	0	0	1	0
9	0	0	1	0	0
10	0	0	1	0	0
11	0	0	1	1	0
12	1	0	1	0	4
13	1	0	1	1	4
14	1	0	1	1	4
15	1	1	0	0	0
16	0	0	0	1	0
17	0	0	1	0	0
18	0	0	1	0	0
19	0	0	1	1	0
20	0	0	1	0	0
21	0	0	1	1	0
22	0	0	1	1	0
23	0	1	0	0	-4
24	0	0	1	0	0
25	0	0	1	1	0
26	0	0	1	1	0
27	0	1	0	1	-4
28	1	0	1	1	4
29	1	1	0	1	0
30	1	1	0	1	0
31	1	1	0	1	0

Relationship Between Approximated (O0 2) & Accurate Output (O2, O1 And O0)

X[4:0]	O'_2	O_2	O_1	O'_1	O'_0	Error Distance
9	0	0	1	0	0	-2
10	0	0	1	0	0	-2
12	0	0	1	0	0	-2
15	0	1	0	1	0	-2
16	0	0	0	1	1	2
19	1	0	1	0	1	2
21	1	0	1	0	1	2
22	1	0	1	0	1	2

Error Cases and Distance of Design 2

Design 3

In this design, only output O1 is replaced by O0 1. Expression for O0 1 is given below. Remaining outputs of the compressor (O0 and O2) are kept same as original expression. The pass rate of the compressor is 75% and error distance is either +2 or -2. In this design, the critical path has three XOR, two AND, one OR and one inverter gates. Figure 4 shows the logic diagram of output O0 1 in design 3 approximate compressor.

$$O_1' = X_4 \oplus [X_0 \cdot (\sim(X_0 \oplus X_1)) + (X_2 \cdot (X_0 \oplus X_1))]$$

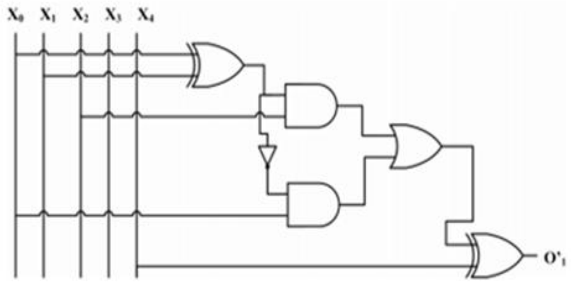


Fig 4: Logic diagram of output O0 1

Design 4

In this design, output of O1 expression is approximated (O0 1) and expressions for O0 and O2 are kept as an accurate. Expression for approximated O0 1 is given below. O 0 1 = X2 ⨁ X3 (9) only one X-OR gate is utilized to get approximated O0 1. The length of the critical path is same as design 3. This consumes the lesser area and power than the other proposed 5-3 compressor designs. But the pass rate of this compressor is 62.5% and the maximum error distance is either +2 or -2.

Design of 15-4 Compressor

This section describes the layout of 15-4 compressor using approximate five-three compressors. The 15-4 compressor become proposed in [12] as shown in figure 5. This compressor has fifteen inputs (X0 - X14) and it produces 4 outputs (O0 - O3). This compressor has five full adders at the beginning degree, two 5-3 compressors in 2nd degree and final level has parallel adder. Each full adder gets 3 primary inputs and it generates "Sum" and "Carry". "Sum" of all complete adders is given to the five-three compressor. Similarly, "Carry" of all full adders is given to some other 5-3 compressor. Outputs of the five-three compressors are given to the parallel adder. Parallel adder is used to generate the final output. In approximate 15-4 compressor, in place of using correct 5-3 compressors, we've used proposed approximate five-three compressors. Full adders and parallel adders are stored as authentic adders in proposed 15-4 compressor. Four approximate designs of 15-4 compressor are proposed. 5-3 compressors are utilized in first 3 designs of approximate 15-4 compressor which makes use of the layout 1, 2 and three of proposed approximate 5-3 compressor. Design 1 and layout four of proposed approximate five-three compressor are used in layout 4 of 15-4 compressor. Design 1 approximate five-three compressor is used to deal with "bring" alerts due to the fact output "carry" has greater than "sum". Moreover, a pass price of design 1 compressor is higher than layout four. Design four approximate 5-3 compressor is used to address sum alerts.

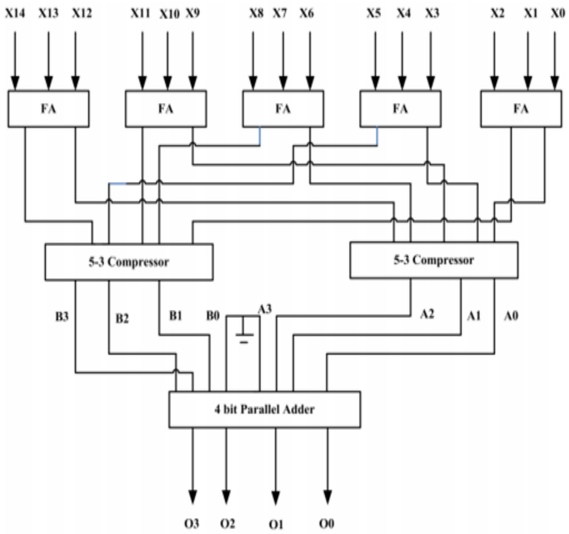


Fig 5: Design of Proposed 15-4 Compressor

Multiplier Design

In this segment, layout of 16 × 16 multiplier is supplied. Four approximate multipliers are designed the usage of the proposed four 15-4 compressors. In addition to this, one accurate multiplier and four other approximate multipliers are taken into consideration. Approximate multipliers using the proposed approximate 15-4 compressors are compared with the accurate sixteen × sixteen multipliers with accurate 15-4 compressors and additionally with other multipliers designed the usage of diverse different approximate compressors. Figure 6 shows the layout of 16 × 16 bit multiplier using 15-4 compressor in which, every dot represents one partial product. Six 15-4 compressors are used to layout one multiplier in the partial product discount and ultimately four multipliers are designed. In determine, square containers indicate using 15-4 and 4-2 compressor inside the multiplier. 15-4 compressors are used within the multiplier from thirteenth column onwards. Column range 13 of the multiplier has only13 partial merchandise. Two zeros are added in that column to make use of the 15-4 compressor. Similarly, one "0" is delivered in 14th column. Along with 15-4 compressors inside the multiplier different accurate compressor like 4-2 and half of, full adders are used for partial product discount. Approximate compressors are used in 13th, 14th and 15th column of multipliers. Use of approximate compressors in most full-size element could produce a larger error price. Design 1 of 15-4 approximate compressor is used in multiplier 1. Similarly, layout 2, 3 and 4 of 15-four approximate compressors are utilized in multiplier 2, three and four respectively. In accurate multiplier, all correct 15-4 compressors are used at the side of correct 3-2 and 4-2 compressors. Accurate four-2 compressors, half and full adders are used in 2d and 1/3 stage of partial product reduction tree. In very last stage, parallel adders are used to compute the very last end result.

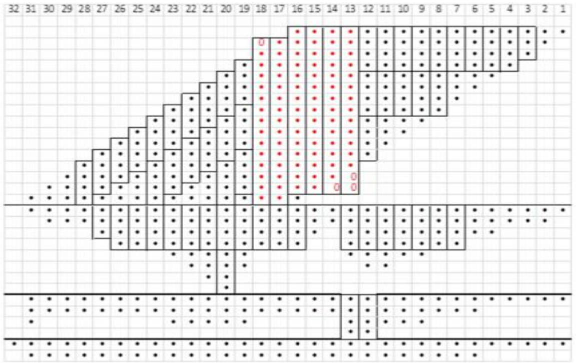


Fig 6: Design of 16 × 16 Multiplier Using 15-4 Compressor

4 Bit Parallel Adder

The 4 bit parallel adder perform operations on two 4-bit binary numbers B4 B3 B2 B1 and A4 A3 A2 A1 are to be added with a carry input C1. This can be done by cascading four full adder circuits as shown in Figure 7. The least significant bits A1, B1, and C1 are added to the produce sum output S1 and carry output C2. Carry output C2 is then added to the next significant bits A2 and B2 producing sum output S2 and carry output C3. C3 is then added to A 3 and B 3 and so on. Thus finally producing the four-bit sum output S4 S3 S2 S1 and final carry output Cout.

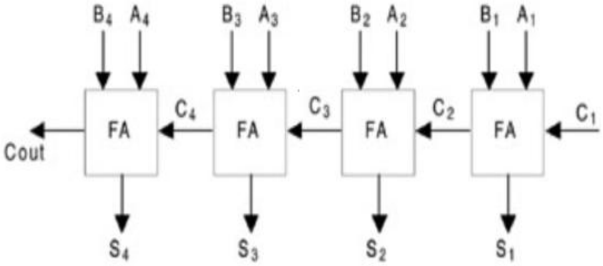
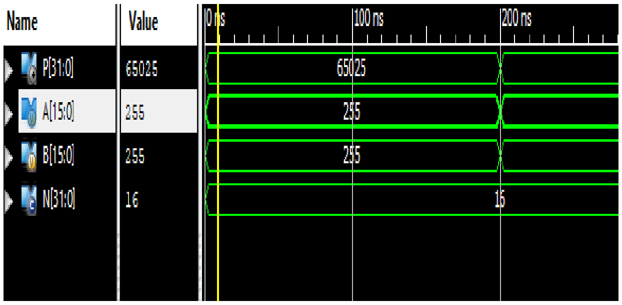


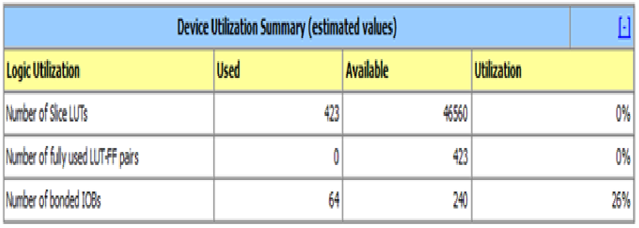
Fig 7: Block Diagram of 4 Bit Parallel Adder

V SIMULATION RESULTS



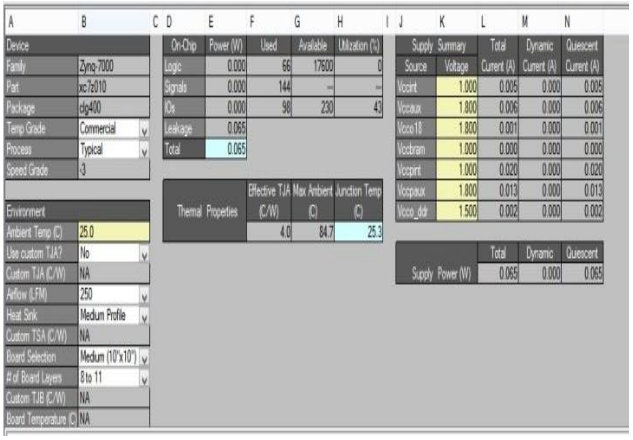
Name	Value
P[31:0]	65025
A[15:0]	255
B[15:0]	255
N[31:0]	16

Design Summary:



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	423	46560	0%
Number of fully used LUT-FF pairs	0	423	0%
Number of bonded IOBs	64	240	26%

Power Summary:



Device	
Family	Zynq-7000
Part	xc7z010
Package	clg400
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	8 to 11
Custom TJB (C/W)	NA
Board Temperature (C)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	66	17600	0
Signals	0.000	144	---	---
IOs	0.000	98	230	43
Leakage	0.065			
Total	0.065			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.0	84.7	25.3

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.005	0.000	0.005
Vccaux	1.800	0.006	0.000	0.006
Vcco18	1.800	0.001	0.000	0.001
Vccbram	1.000	0.000	0.000	0.000
Vccpint	1.000	0.020	0.000	0.020
Vccpaux	1.800	0.013	0.000	0.013
Vcco_ddr	1.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.065	0.000	0.065

The above result represents the synthesis implementation by using the Xilinx ISE software. It indicates very less area and power was used for the proposed design.

VI CONCLUSION

This paper shows the four designs of approximate 15-4 compressor. 16 × 16 bit multipliers are designed by using those proposed 15-4 compressors. Approximate multipliers provide better performance than existing multipliers with compromising of error rate. Moreover, we have achieved high pass rate and the normalized error distance value of multipliers designed using proposed 15-4 compressor is very small. In order to validate our work, image contrast has been performed with the help of proposed multiplier. The quality of the processed image shows that our proposed multipliers are working fine. The PSNR (Peak Signal to Noise Ratio) value of other approximate multiplier is less than 10 dB, but in our proposed multiplier it provides greater than 30 dB, which is sufficient for most of the image processing applications. The proposed multipliers (3)-(6) are suitable for image processing applications whereas, multipliers (7)-(9) can be used where circuit performance is complex. Researchers can choose the multipliers based on their applications. Finally, our proposed multipliers consume low power and capable of giving the good result in terms of pass rate and error distance.

VII FUTURE SCOPE

Redundant basis (RB) multipliers over Galois Field have won large recognition in elliptic curve cryptography (ECC) mainly because of their negligible hardware cost for squaring and modular reduction. In this paper, we have proposed a singular recursive decomposition algorithm for RB multiplication to gain high-throughput digit-serial implementation. Through efficient projection of signal-flow graph (SFG) of the proposed set of rules, a highly regular processor-space flow-graph (PSFG) is derived. By figuring out suitable cut-units, we have modified the PSFG certainly and accomplished efficient feed-forward cut-set retiming to derive 3 novel multipliers which not only contain considerably less time-complexity than the existing ones but additionally require less place and much less power intake compared with the others. Both theoretical evaluation and synthesis results verify the efficiency of proposed multipliers over the present ones.

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