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DESIGN OF AREA EFFICIENT AND LOW POWER 4-BIT MULTIPLIER BASED ON TG

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Abstract:- With the rapid advancement in technology, a wide range of high speed mobile computational devices and equipment's are being introduced in the market. These computational devices strain and drain the battery very quickly. Researchers are making efforts to find ways and means to conserve the battery power for longer period. The core key components in these computational devices are the Adders and Multipliers to support high speed computationally intensive applications in real time. Thus, it becomes more important to reduce power dissipation and area in these Adders and multiplier modules as they affect the performance of the device. This paper presents a design of 4-bit multiplier using full adder cell based on transmission gate adder technique. The proposed adder design consists of a smaller number of transistors compared with full swing gate distribution technique. Therefore, the complete design of the complete adder dissipates the reduced power, while improving the area and ensuring a complete output voltage. The fully proposed adder used to design the Array, Baron and Baugh Wooley multipliers, the power and transistor number of these multipliers has improved compared to the full swing gate diffusion technique.

Keywords— *FS XOR-XNOR; FS-GDI; Full Adder; Multiplier; MUX; GDI.*

I INTRODUCTION

IC designers face new challenges due to the exponential growth of electronic devices and equipment in recent years. Adding additional functionality along with real-time applications requires a revolutionary change in the chip design process. The increasing demands on single-chip computing require the development of sophisticated tools that can perform complex operations, which also increases computing power. Therefore, the development of high-speed computing equipment, that is, adders and multipliers, is a major challenge in the current scenario. For low power real-time applications, computational-intensive digital signal processing algorithms are implemented in specialized VLSI systems. The multiplier is one of the most important parts of these systems. The processing speed of the processor is highly dependent on these arithmetic devices. High-performance processors complicate design. To improve the performance of the processors, the complexity of such arithmetic devices must be increased. Recent developments in portable electronic devices and digital signal processing systems require flexible computing power, low power consumption, and shorter design cycles. The two most important design criteria that determine processor performance are speed and power consumption. As shown, much research has been done in the literature to provide energy efficient multiplier and adder architectures. Modern developments are focused primarily on reducing the silicon area, but in the last decade the emphasis has shifted primarily to speed and power. The complexity of the design directly depends on the speed of calculation. The high speed requirement leads to greater circuit complexity, so more transistors will be required in the design, which will also lead to a large power dissipation. Hence, there is a trade-off between speed and power dissipation. The adder is the building block of any computing equipment. Therefore, its performance directly affects the operation of the entire system. Therefore, improving the performance of the adder architecture is a top priority. External or internal methods can be used to improve the overall performance of any system. External methods deal with the characteristics of the input data, while

internal methods deal with the logic, circuitry, and architecture of the multiplier. The basic element of the multiplier design is the summing cell, which significantly affects the overall performance of the multiplier.

II.EXISTING METHOD

Multipliers are an integral part of major application systems such as Digital Signal Processor (DSP), microprocessors, and application-specific integrated circuits (ASIC's), and they play a major role in the public domain, power consumption, and processor performance. Multiples that use less power, and take up less space, are required. The primary components of multiples are AND gates, Full Adders, and Half Adders. To improve system performance, these circuits should be improved. Addition is the basic process of any digital system. The efficient performance of additional functions plays a significant role in engineering more complex structures such as arithmetic logic units for microprocessors. The arithmetic accounts are covered under the logical levels while the area and other factors are covered under the circle levels. Hence, we design an input snake for full swing gate propagation.

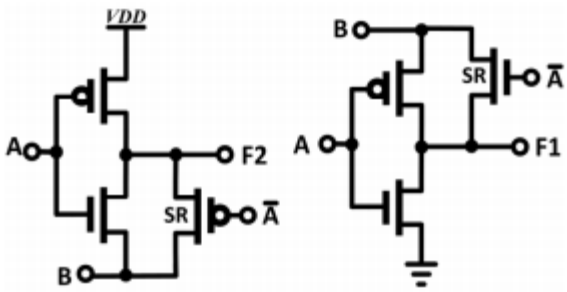

Fig. 1. FS GDI cell (a) F2, (b) F1

Full adder:

The proposed design consists of 18 transistors to realize a complete 1-bit snake as shown in the fig. In block 1, an XOR operation is performed between inputs A and B. Where, as in block 2, an XOR operation is performed between the output of block 1 and X. And then the final result is obtained. Finally, the load output is generated from block 3, where Cin and A are received as inputs and the output of block 1 is set as the multiplexer select line.

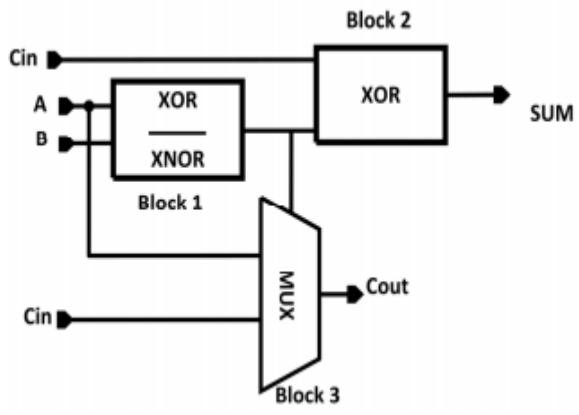

Fig. 2. Block Diagram of Proposed Full Adder

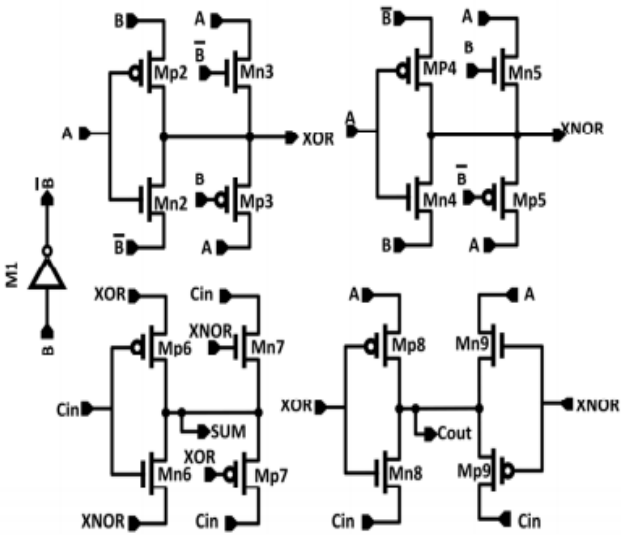

Fig. 3. Proposed design for 1-Bit Full Adder

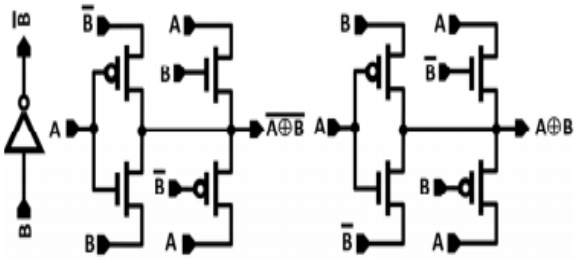

Fig. 4. GDI cell; (a) 6T-XNOR Gate, (b) 6T-XOR Gate

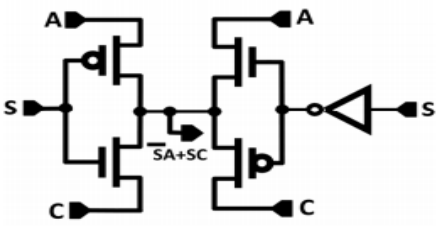

Fig. 5. FS-GDI MUX

III.PROPOSED METHOD:

Transmission gate or pass gate act as a simple switch circuit and present a new class of logic circuits that used pass transistors or TG as a basic building block. As shown in Fig 6, the CMOS transmission gate consists of one PMOS and one NMOS transistor, connected in parallel. The gate voltages applied to these two transistors as complementary signals. As such, the CMOS TG operates as a bidirectional switch between the nodes A and B which is controlled by signal C. If the control signal C is equal to VDD, then both transistors are turned on and provide a low-resistance current path between the nodes A and B. If, on the other hand, the control signal C is low, then both transistors will be off, and the path between the A and B will be an open circuit. Fig 6 also shows three other commonly used symbolic representations of the TG.

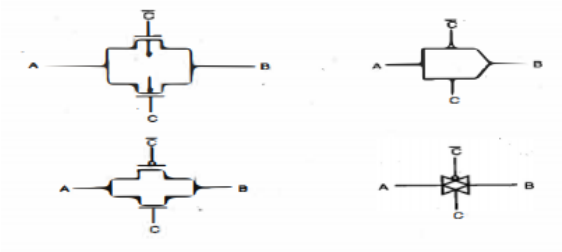

Fig. 6. Basic Transimission Gate

The designs of a transmit gate adder use complementary properties of the pull-down and pull-up transistor. It has 20 transistors. This TGA (Transmission Gate Adder) is built by a parallel connection of PMOS and NMOS transistor. And the operation of the circuit is controlled by complementary signals. Since it has fewer transistors compared to the gate diffusion input adder, it has less area and power consumption. The full adder circuit diagram of the transmit gate is shown below.

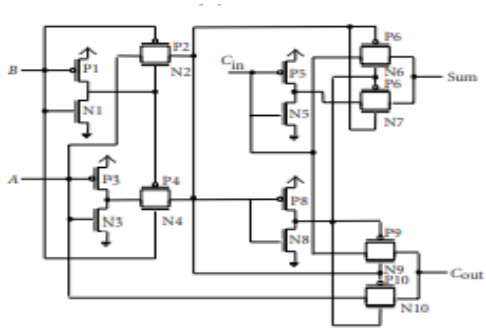

Fig. 7. Proposed design for 1-Bit Full Adder

Array Multiplier:

The Array multiplier is the simplest parallel multiplier structure. This multiplier uses a standard add and shift operation based on "add and shift" algorithms to perform the multiplication operation. The structure of a 4-bit matrix multiplier is shown in Fig. 9. The partial product generator consists of n numbers of “Y” gates to multiply the multiplier by each bit of the multiplier, and then these partial products are shifted according to their order, and this addition operation can be performed using a full and half adder. adder. In a 4x4 matrix multiplier, AND 4x4 elements are used to generate partial products and 4x (4-2) full adders and 4 half adders to generate.

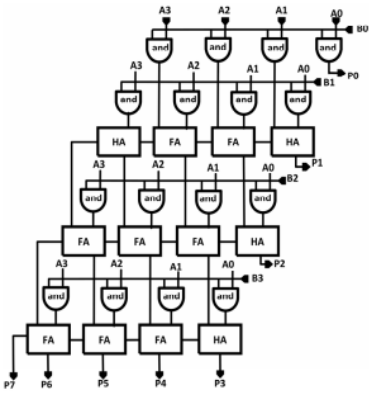

Fig. 8. 4x4 Array Multiplier

Braun Multiplier:

The Braun Multiplier is a linear factor that has a regular structure and is known as a carry-preserving matrix factor. This multiplier operates on the basis of the fact that it does not immediately add the "carry bits" that are output from the first stage, but is stored for the next stage of addition. As shown in Figure 10. Braun multiplier 4x4 consisting of (4-1) rows of carry and store adders (CSAs) and (4-1) bit ripple carry adders in the last row, and each row contains (4-1) full adders (FAs). The main advantage of the Braun multiplier is that it has only one critical path instead of many of the paths found in the matrix multiplier, and it is most widely used in DSP applications due to its low power consumption.

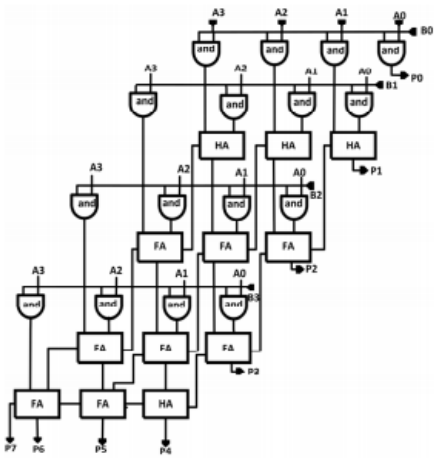

Fig. 9. 4x4 Braun Multiplier

Baugh Wooley Multiplier:

A Baugh Wooley multiplier based on parallel array architecture. This multiplier is used for both unsigned and signed number multiplication. Signed number operands which are represented in 2's complemented form to make sure that the signs of all partial products are positive. The 4x4 Baugh Wooley multiplier is shown in fig. 9.

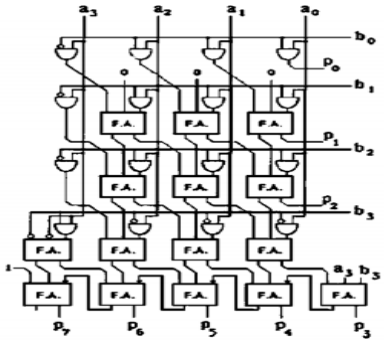

FIG. 10. 4X4 Baugh Wooley Multiplier

IV.RESULTS

The proposed full adder is designed and using this full adder, we are designing the Array, Braun and Baugh wooley Multiplier and simulations are performed in TANNER EDA tool.

Simulated Wave form of Proposed Full Adder:

The simulated waveforms are obtained by assigning the input values at various levels of extraction and the corresponding outputs are obtained from the assigned inputs. The outputs obtained are complementary with respect to the corresponding complementary inputs. The simulated waveforms of the proposed work are shown here. Figure shows the simulated output of Proposed Full adder. Output are realized based on the logic design of the Full adder which is verified.

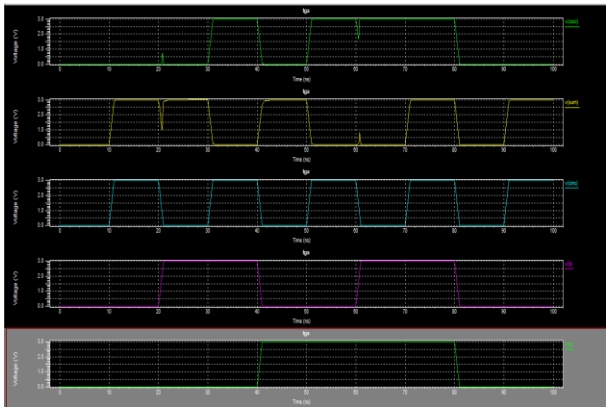

Fig:11 Waveform of proposed Full Adder

Table:1

Name of adder	Area	Power	Delay
GDI Adder	22	53.6uw	10ps
TGA Adder	20	42.2uw	14ps

Simulated Wave form of Proposed Array Multiplier:

The simulated waveforms are obtained by assigning the input values at various levels of extraction and the corresponding outputs are obtained from the assigned inputs The simulated waveforms of the proposed work are shown here. Figure shows the simulated output of Array Multiplier using Proposed Full adder.Output are realized based on the logic design of the Array Multiplier using Proposed Full adder which is verified.

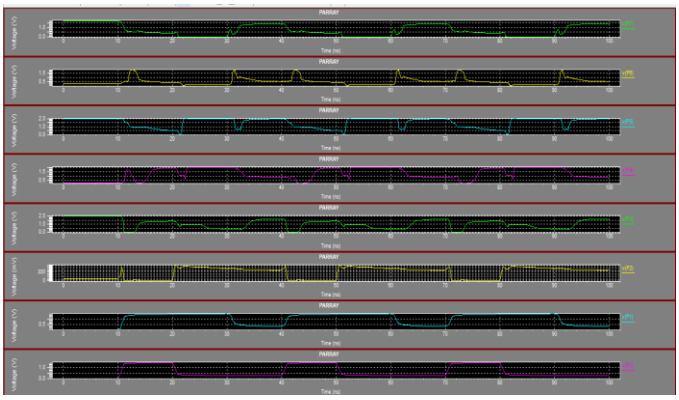

Fig:12 Waveform of Array multiplier using proposed Full Adder

Simulated Wave form of Proposed Braun Multiplier:

The simulated waveforms are obtained by assigning the input values at various levels of extraction and the corresponding outputs are obtained from the assigned inputs The simulated waveforms of the Proposed work are shown here. Figure shows the simulated output of Braun Multiplier using Proposed Full Adder. Output are realized based on the logic design of the Braun Multiplier using Proposed Full adder which is verified.

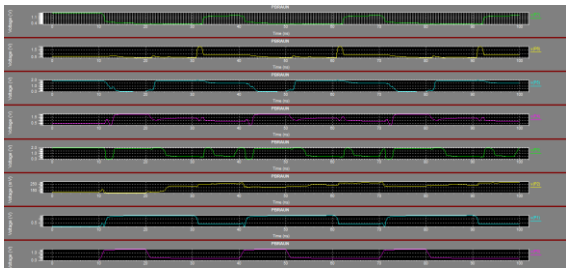

Fig:13. Waveform of Braun Multiplier using proposed Full Adder

Simulated Wave form of Proposed Bough Wooley Multiplier:

The simulated waveforms are obtained by assigning the input values at various levels of extraction and the corresponding outputs are obtained from the assigned inputs .The simulated waveforms of the existing work are shown here. Figure shows the simulated output of Baugh Wooley Multiplier using Proposed Full Adder. Output are realized based on the logic design of the Baugh Wooley Multiplier using Proposed Full adder which is verified.

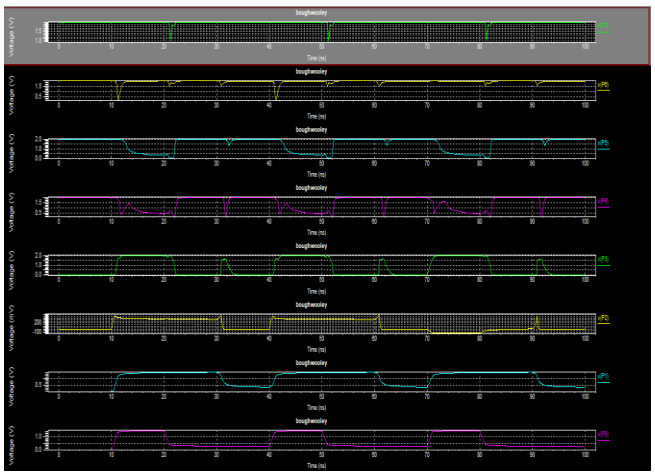

Fig:14. Waveform of Baugh Wooley Multiplier using proposed Full Adder

Table:2

Name of multiplier	area	Power
Existing Array	**248**	**2.3mw**
Proposed Array	**232**	**1.9mw**
Exising Braun	**248**	**1.9mw**
Proposed Braun	**232**	**1.5mw**
Existing Bough Wooley	**374**	**2.4mw**
Proposed Bough Wooley	**344**	**1.0mw**

V.CONCLUSION

A transmission gate full adder has been designed that is efficient in both area and energy compared to the full revolving gate broadcast input technique adder. Using this proposed adder, the Array multiplier, the Braun multiplier, and the Baugh Wooley branch multipliers are designed. Since the transmission gate full adder requires fewer transistors compared to the full revolving gate diffusion full adder, the area and power dissipation of the three designed multipliers are also effectively reduced.

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