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DESIGN OF N-BIT ALU USING QUANTUM DOT CELLULAR AUTOMATA BASED SELF CORRECTION

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Abstract: The New Technology is quantum dot cellular automata was developed at Nanoscale level, which required less area by utilizing quantum cells compared to CMOS technology thus it consumes low power. The CMOS based Transistors can reduce their channel width at only certain levels than their present size .The QCA approach tends to one of the best arrangements in beating this physical width and channel width at molecular level. We can perform any Digital Logic Function, with the avail of QCA based majority gates. In this paper fast adders like Ripple carry adders(RCA) Ripple carry subtractors and Array multipliers of N-bit size operations are performed by utilizing Majority gates that has all best in class contenders and accomplishes the best area-delay tradeoff, delay (speed), power utilization and PDP.

Keywords - Adders, quantum-dot cellular automata (QCA), Delay, power consumption, Majority gates (MG).

I INTRODUCTION

There are two vigorously irrelevant approaches of two electrons in the QCA cell for an evacuated cell, expected cell polarization P=+1 and cell polarization P=-1.while Cell polarization P=+1 alludes to parallel 1 while cell polarization P=-1 alludes to relating 0.In expansion, this thought is graphically potrayed in figure - 1.It is additionally colossal that there is an unpolarized state as well. In an unpolarized state, potential points of confinement between contact are diminished which diminishes the exhibit generally zero polarization and the two electron wave limits have been delocalized over the telephones appeared in Figure 1

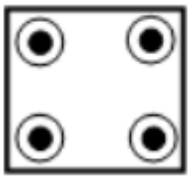


Fig 1.unpolarized cell

The numbering of specks signified by electrons in the cell goes clockwise beginning from the matrix on the upper appropriate with quantum level I =1, base right cell I =2, base left cell I =3, and upper left cell i=4. The polarization level P in a cell is characterized as Where Pi means the electronic charge at speck current. The polarization estimates the charge design for example the degree to which the electronic charge is appropriated among the four cells.

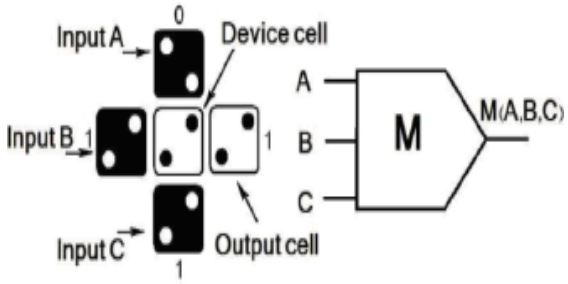


Fig 2.Majority gate using QCA

The basic QCA sensible circuit is the three-input majority gate(MG) that shows up in Figure 2 from which progressively complex circuits can be fabricated. The fundamental MG gates are acquired by setting four neighboring cells bordering to a quantum cell, which is in the center. Three of the side cells are utilized as data sources, while the staying one is the yield. The quantum cell will consistently expect the majority polarization is where there will be at least charge between the electrons in the three information cells and the quantum cell.

Consider the coulombic interface between cells 1 and 4,cells 2 and 4,cells 3 and 4 to perceive how the contraption cell accomplishes its most minimal imperativeness state (and from now on P=+1 in figure2).Typically, coulombic association between electrons in cells 1and 4 would make 4 change its polarization in light of electron stun. (expecting cell 1 is a data cell). In any case, cells 2 and 3 in like manner sway the polarization of cell 4 and have polarization

P=+1. Along these lines, in light of the way that the greater part of the cells influencing the contraption cell have polarization 1 P , it additionally will moreover expect this polarization because the forces of Coulombic association are more grounded for it than for 1.

II. LITERATURE SURVEY

In current years, a variety of structures have acquainted with improve the productivity of the Nano calculator. In any case, there are just a couple of structures that have been proposed for QCA based ALU [1] incorporate adders, multiplexer with the detail of their plans. In addition, QCA Adder is a significant block in the calculation units since multiplication and subtraction tasks can be helped out through the progressive sum activity and two's supplement, separately. Different structures have displayed for QCA adder, which characterized into the single layer [2]–[4] and numerous layer plans. The current multiplexers can be arranged into the single layer [5]–[7] and multilayer circuits. Lamentably, the greater part of the existing methods of the Nano-calculator structures have not clear the important data about their plans, for example, the quantity of quantum cells, No. of MG gates, area and power consumption.

The Figure 3 represents the 1 bit full adder operation, which is implemented by using majority gates of 3 input and 5 input which is considered from literature [2]. To design the full adder they used the following equations

$$C_o = M_3(A, B, C_{in})$$

$$S = M_5(A, B, C_{in}, C_o', C_o')$$

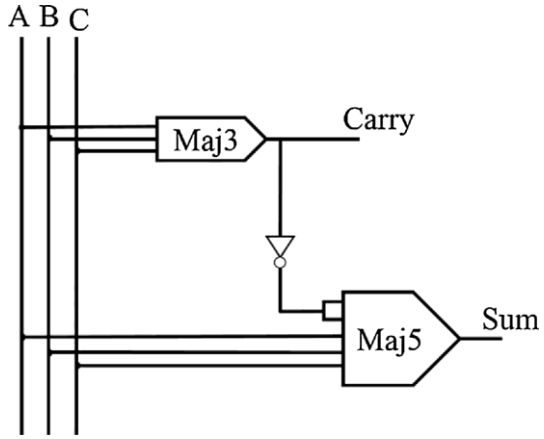


Fig. 3 Schematic of Existing Full adder

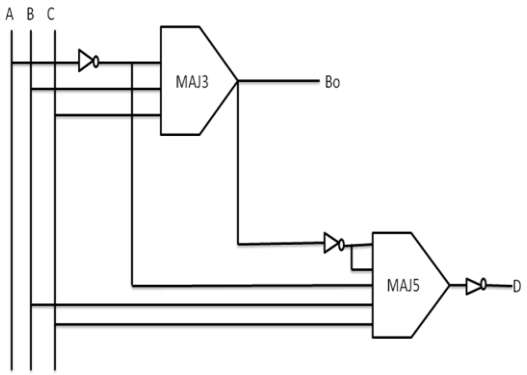


Fig. 4 Schematic of Existing Full Subtractor

A full subtractor is utilized to plays out the subtraction opeartion of three inputs A,B and C. The two yields of subtractor circuit are difference 'D' and borrow 'B'. To execute full subtractor in QCA it required the inverters as far as MGs, which can be given by

$$B_o = M_3(A', B, C)$$

$$D = M_5'(A', B, C, B_o', B_o')$$

The schematic depiction of full subtractor circuit is appeared by Fig.4. The utilization of 5-input MGs make the circuit more straightforward than utilizing just 3-input MG and inverter from literature [2].

III PROPOSED METHOD

The major drawback from the above literature is that they consumed the more area, thus they used the more power consumption. The number of majority gates they used to generate the full adder and subtractions are two 3-input Majority gates, two 5-input majority gates And also they required the four inverter gates. To optimize this, A new design has been developed which is works both full adder and full subtractor at a time.

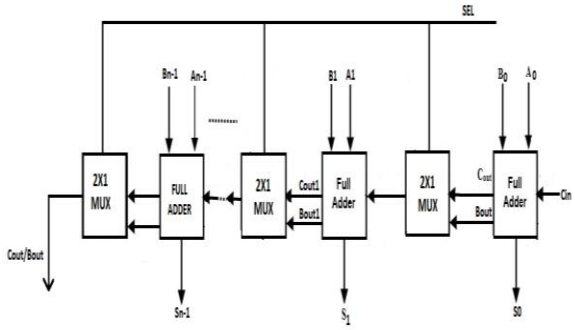


Fig. 5 Schematic of proposed N-bit adder and Subtractor

3.1 PROPOSED ADDERS AND SUBTRACTORS:

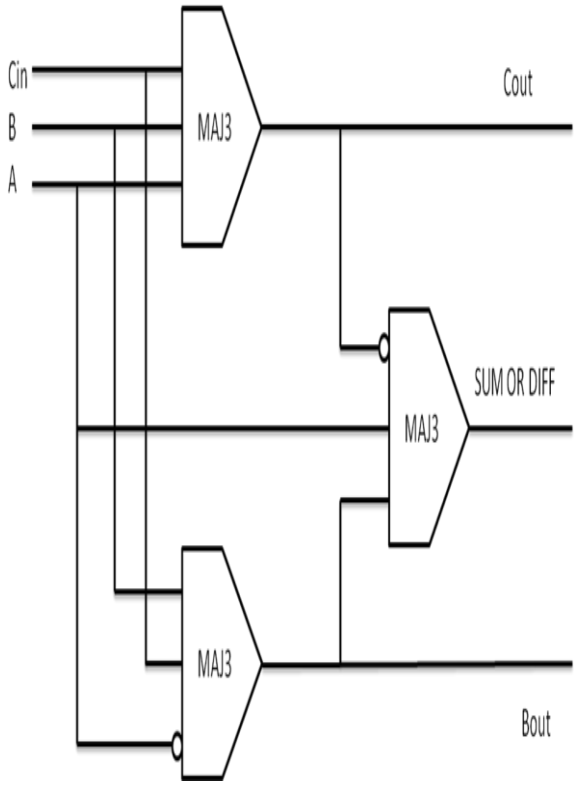


Fig. 6 Schematic of proposed Full adder and Subtractor

The proposed method is implemented with only three 3-input majority gates and two inverters and there is no need of five input majority gates. So the number of quantum cells will reduced in this design method, it causes to reduce the area as well as power.

The above figure represents the Full adder and Subtractor; here the single circuit will perform the both operations. Majority gate M1 will generate the carry out and Majority gate M2 will generate the borrow out. Carry out and Borrow out as well as input A will be applied as inputs to the 3rd majority gate to generate the sum or diff.

The above figure represents the N-bit adder and Subtractor by connecting the series manner of N stages. The each FAFS block represents the fig 5 with the majority logics. Here, the carry out and borrow out of the first FAFS block will be applied as input to the next stage. If we required adder as the functionality then carry out will be applied as carry in by making the selection line of 2to1mux to zero, If we required subtractor as the functionality then borrow out will be applied as carry in by making the selection line of 2to1mux to one. The mux operation using majority gates will be explained in this paper in further chapters.

3.2 PROPOSED MULTIPLIERS

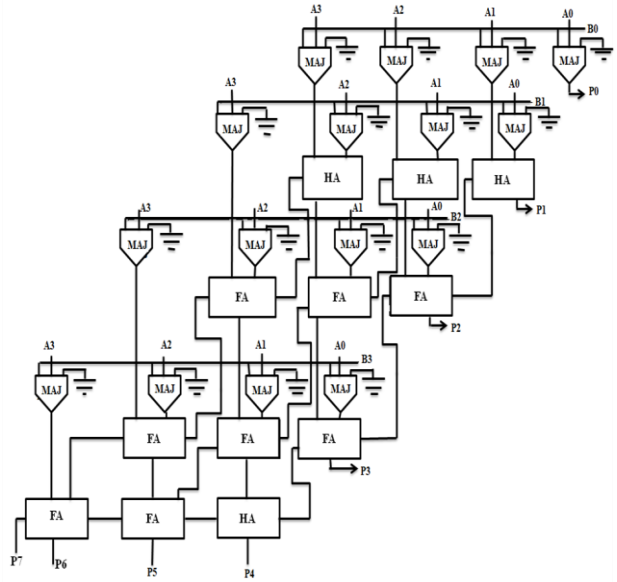


Fig. 7 Schematic of 4x4 Barun Multiplier

The above figure performs the 4 bit multiplication operation between A,B. Initially, 16 partial precuts namely A0B0, A1B0, A0B1 and so on generated by using bitwise Majority gates operation between A,B and ground. By making any one of the input zero in the majority gate it will act as the AND gate. For implementing the half adder, by making the anyone of the input in Full-adder zero and the Full adder circuit is represented in Fig 5.

For develop the N-bit multiplier, it needs 4 Nby2 multipliers. For example, for implementing 8 bit multiplier it requires four 4-bit baurn multipliers. Here, three N-bit Ripple carry adders are used as developed in fig. 7 in this paper. First adder adds the outputs of second and third multiplier partial products here, and addition output will forward to second stage adder. First Nby2 baurn multiplier half of the lsb output bits fed as the final outputs, next half msb output bits fed as the input to the second stage adder. in order to avoid the size of array mismatches Nby2 zeros added to second and third stage adders. After completing the all successful addition product P will generate.

3.3 LOGICAL UNIT

As part of the logical unit here we are considered either AND operations and OR operations. By making anyone of input zero in majority gate it will act as the AND gate and similarly by making anyone of input or in majority gate it will act as the OR gate. Inversions of AND, OR gate will create the universal gates like

NAND and NOR gates. In the, The FAFS deisgn it has SD pin as three input XOR function, and inversion of it creates XNOR gate.

3.4 ALU:

The proposed ALU performs four operations between inputs A and B. when multiplexer selection lines S0 and S1 becomes {0, 0}, it will functions as Adder, similarly for {0,1}functions as subtractor, for {1,0} functions as multiplier and for {1,1} act as logical unit.

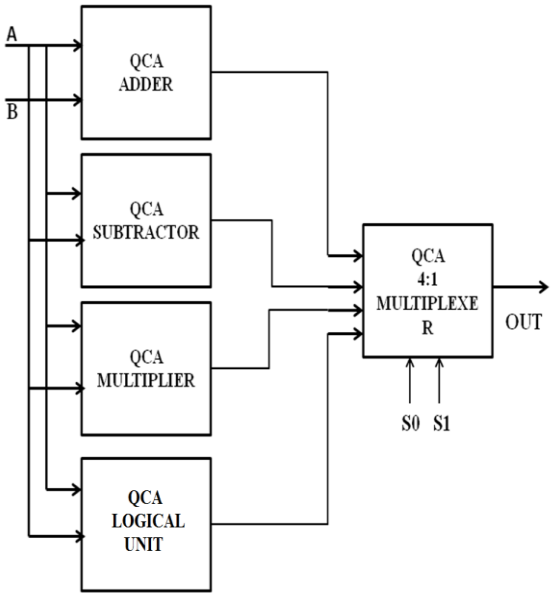
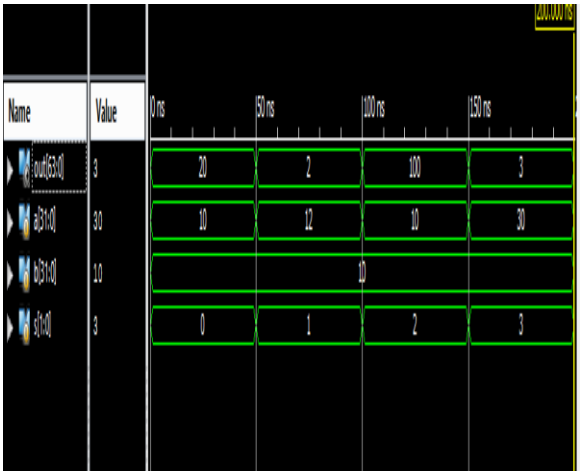


Figure 8: Block diagram of ALU

IV . SIMULATION RESULTS:

4.1 WAVEFORMS



The above result represents the simulation waveform by using the Xilinx ISE software. Where S is the selection line, if s is 0 then a,b {10,10}added generates the output as 20, s is 1 then a,b {12,10}subtracted generates the output as 2, s is 2 then a,b {10,10}multiplied generates the output as 100 and s is 3 then a,b {30,10}logical unit generates the result as 3.

4.2 DESIGN SUMMARY

parameter	EXISTING METHOD[1]	PROPOSED METHOD
Time delay	59.110 ns	54.238 ns
Power utilized	1.293uw	0.143uw
Look up tables	5277	4982

The above result represents the synthesis implementation by using the Xilinx ISE software. From the above table, it is observed that only 4982 look up tables are used out of available204000. It indicates very less area (2%) was used for the proposed design.

4.3 TIME SUMMARY

```
LUT2:I0->O            1   0.043   0.000  div1/Madd_GND_49_o_GND_49_o_a
MUXCY:S->O            1   0.230   0.000  div1/Madd_GND_49_o_GND_49_o_a
XORCY:CI->O           2   0.251   0.347  div1/Madd_GND_49_o_GND_49_o_a
LUT4:I2->O            1   0.043   0.000  div1/Msub_n0258_Madd_lut<30>
MUXCY:S->O            0   0.230   0.000  div1/Msub_n0258_Madd_cy<30> (
XORCY:CI->O           1   0.251   0.289  div1/Msub_n0258_Madd_xor<31>
LUT5:I4->O            1   0.043   0.279  Mmux_out110 (out_0_OBUF)
OBUF:I->O                 0.000          out_0_OBUF (out<0>)
----------------------------------------
Total                          54.238ns (31.895ns logic, 22.343ns route)
                                        (58.8% logic, 41.2% route)
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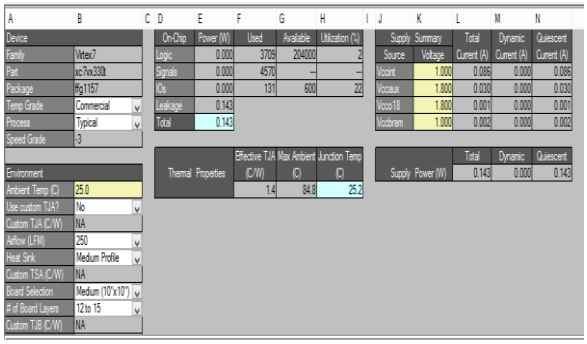
The above result represents the time consumed such as path delays by using the Xilinx ISE software.the consumed path delay is 54.238ns.

4.4 POWER SUMMARY



The above result represents the power consumed by using the Xilinx ISE software. The consumed power is 0.143uw.

V CONCLUSION

In this paper, a new QCA based N-bit adder's, subtractions and multipliers designs has developed to perform the arithmetic and logical operations. The simulation outcome confirms the proposed operations

have developed with less cells, area and latency. In addition, to decrease the complication of the addition associated operations, an proficient adder-subtractor has been proposed.

REFERENCES

[1] Chakrabarty, Ratna, et al. "Nano-Calculator using Quantum Dot Cellular Automata (QCA)." 2017 1st International Conference on Electronics, Materials Engineering and Nano-Technology (IEMENTech). IEEE, 2017.

[2] M. Balali, A. Rezai, H. Balali, F. Rabiei, and S. Emadi, "Towards coplanar quantum-dot cellular automata adders based on efficient three-input XOR gate," Results Phys., vol. 7, pp. 1389–1395, 2017.

[3] S. K. Iakshmi, G. Athisha, M. Karthikeyan, and C. Ganesh, "Design of subtractor using nanotechnology based qca," in Communication Control and Computing Technologies (ICCCCT), 2010 IEEE International Conference on. IEEE, 2010, pp. 384–388.

[4] H. Cho and E.E. Swartzlander, Jr., "Serial Parallel Multiplier Design in Quantum-Dot Cellular Automata," Proc. 18th IEEE Symp. Computer Arithmetic, pp. 7-15, 2007.

[5] M. Naji Asfestani and S. Rasouli Heikalabad, "A unique structure for the multiplexer in quantum-dot cellular automata to create a revolution in design of nanostructures," Phys. B Condens. Matter, vol. 512, no. January, pp. 91–99, 2017

[6] M. G. Waje and P. K. Dakhole, "Design and implementation of 4-bit arithmetic logic unit using Quantum Dot Cellular Automata," 2013, pp. 1022–1029.

[7] Sasamal, T. N., Singh, A. K., & Ghanekar, U. (2016). Design of non-restoring binary array divider in majority logic-based QCA. Electronics Letters, 52(24), 2001–2003.